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Design of 2.4-2.5 GHz CMOS LNA
with low DC Power Consumption and 1.98 dBm Noise Figure

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***Abstract*— In this paper a CMOS LNA which fabricated with the 0.13um CMOS process is proposed. The arnplifier is optimized for Bluetooth applications operating in the 2.4 - 2.5GHz band. The inductive degeneration topology used in the LNA provides low noise, high gain and a large IIP3. The LNA consists of two amplifying stages with on-chip inductors and capacitors. Simulation was made by using the ADS software. The proposed LNA consuming 6.11mA current at 1.2V supply voltage, it exhibits a linear gain of 20.343 dB, noise figure of 1.98 dB, input return loss (S11) of -11.11 dB , S12 of -44.69 dB and an IIP3 of 5 dBm .**

Keywords—LNA; Noise Figure; stability ,linearity, IIP3

I. INTRODUCTION

With the rapid development of the communication industry, more and more kinds of wireless communication apparatus are needed, such as small a low noise figure, low input/output return losses, a high IIP3, have been the main target of the businessman and the manufacturer of the wireless communication. In this condition, swift developmental radio frequency (RF) wireless communication technology has been widely used in all fields of the world. Low noise amplifier (LNA) which is in the RF front-end circuit has the great value in this field [1-3]. LNAs are a crucial element of RF receivers. Their role is to amplify the RF signal to a level that meets the sensitivity requirements of the other components (e.g. Filter). In order to achieve the required gain it is essential to make sure that the reflection coefficients S11 and S22 are minimized. In addition, LNAs are usually the bottleneck in terms of Noise Figure and distortion.

In this paper, we describe 2.4-2.5GHz-band CMOS LNAs optimized for Bluetooth application. Our purpose is to improve the performance of LNA. The emphasis of this study is to reduce the power consumption of the CMOS LNA while still retaining acceptable noise performance, good input/ output match, sufficient linearity, and a high dynamic range. A cascode amplifier topology with inductive degeneration at the source was used. The LNA offered NFs of 1.98dB and input return losses of-11dB, output return losses of -44.69dB, input ICP1 of -10 dBm and IIP3of 5dBm with power consumptions of 7.33 mW .

II. INPUT AND OUTPUT MATCHING

It is remarkable that the performance of wireless receiver system is assumed by input matching of LNA, which must be take account of in the design. The topology is matched to a 50 Ω source using the inductive Degeneration Ls. Maximum power transfer from the previous stage (i.e., antenna or duplexer) to the LNA, takes place by minimizing the input return loss. This is often expressed by the parameter S11.The expression of input impedance is defined in (1)

$$Zin=s(Lg+Ls)+1/sCgs+gm/Cgs\ Ls\approx s(Ls+Lg)+1/sCgs+WL \quad (1)$$

to achieve input matching, the Zin should be 50 Ω, so

$$Zin=gm/Cgs\ Ls \quad (2)$$

The value of Ls is picked and the values of gm and Cgs are calculated to give the required Zin.

III. NOISE FIGURE

The noise figure (NF) is used to specify degradation in the signal-to-noise ratio caused by the LNA and it is always expressed in dB. The noise factor NF is the linear equivalent of the noise figure, and it is given by the following expression

NF= (Total output noise)/(Total output noise due to the source) (3)

IV. LINEARITY

Even-order intermodulation products are normally found at frequencies well above or below the signals which generated them and are usually of Iittle concern. The odd-order distortion produced by an LNA can give rise to distortion products which can mask or interfere with the desired signal. The third-order products are the most significant and can lie very close to the signals which generated them in frequency. Third-order non-Linearity is customarily characterized by a specification called the third-order intercept point.

Figure.1. illustrates the relationship between the fundamental and intermodullation distortion products generated by an amplifier for two equal amplitude input signals at different frequencies.

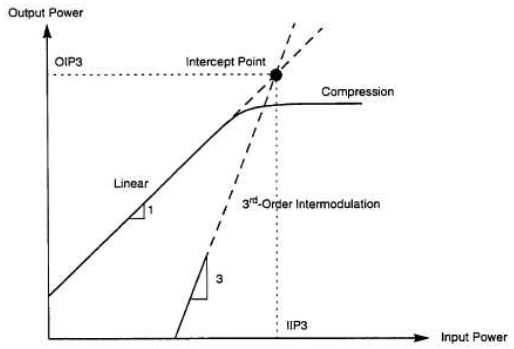

Figure1 amplifier power output versus power input characteristics

V. DESIGN CIRCUIT

Figure 2 shows a schematic of a source–inductor–feedback amplifier with the gate inductor for input impedance matching is shown in Fig. 2. The source inductor is used to achieve simultaneous input and noise matching [4]–[5] and to provide the desired input resistance 50Ω [6]. The cascode structure is a combination of a common–gate load. The Cascode is a combination of a common-source device (ie our LNA) with a common-gate load. This has the effect of increasing the output impedance. The additional cascode device has been configured as a diode .The inductor between the cascode source and supply blocks any RF leaking to the supply rail and maybe varied in value to optimize the gain response of the LNA.

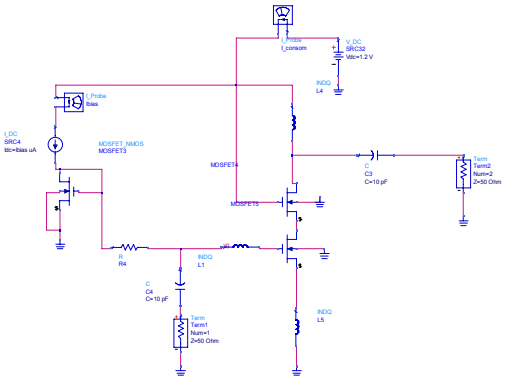

Figure2 Schematic of a source inductive degeneration LNA

VI. SIMULATION RESULTS

ADS simulations for the LNA were done using 0.13 um CMOS process.The amplifier provides a maximum gain of 20.343 dB as shown in figure 3. Cgs and gm are selected according to (1) to make the input matching Zin as possible to 50 Ω. This circuit operated with 1.2 V supply. The reverse isolation S_{12} (Fig.3) is good with more than – 44 dB. A minimum noise figures of 1.98 dB and 3.0 dB are obtained around the desired frequency 2.4-2.5 CHz for the designed LNA's as shown in figure 4.This is due to the use of the cascode configuration. The Simulated results of ICP1 and IIP3 are shown in Figure 6. An input ICP1 of -10 dBm and IIP3 of 5 dBm were obtained.

These results demonstrate that high dynamic range and good linearity have also been achieved. A summary of the simulated amplifier characteristics is also included in Table 1.

From Table I , it is clear that the performance of our CMOS LNA are the best reported values among the 2.4-2.5 GHz band CMOS LNA's compared to some other carachteristic.

According to the meaning of the stability figure K >1 the circuit is stable unconditionally.The stability figure is defined by

$$K = \frac{1 - |S11|^2 - |S22|^2 + |\Delta|^2}{2|S21\,S12|} \qquad (4)$$

$$\Delta = |S11S22 - S12S21| \quad (5)$$

According to (4), when input and output matching are good, decreasing the absolute value of S12 can increase the stability figure K. So according to Figure7, LNA is stable unconditionally.

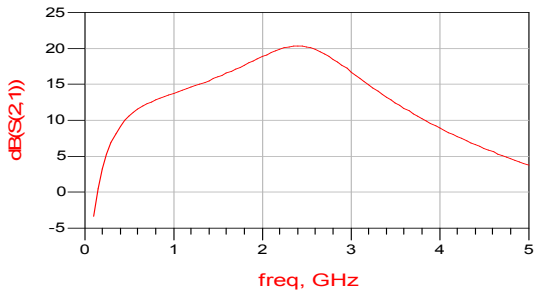

Figure3 Simulated characteristics of gain (S21)

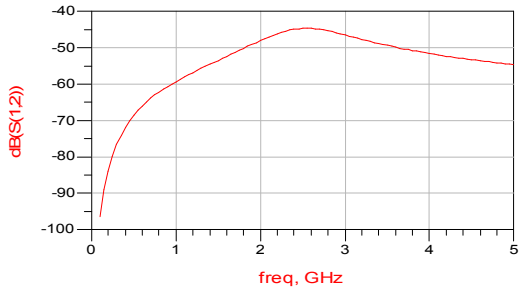

Figure4 Simulated characteristics of reverse isolation (S12)

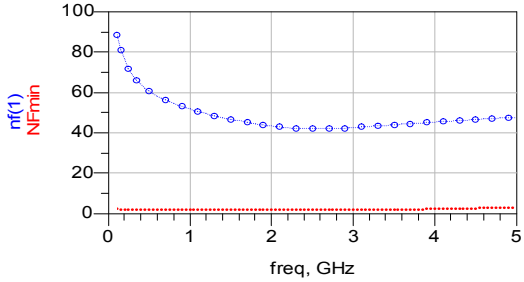

Figure5 Simulated noise figure and minimum NF

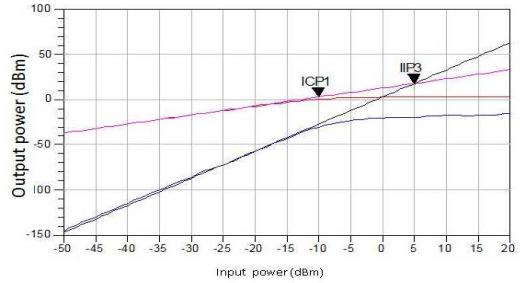

Figure6 Simulated compression point (ICP1) and third-order intercept (IIP3)

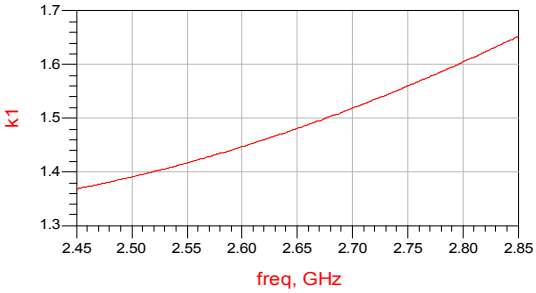

Figure7 Simulated Stability figure K

Table 1 . Classical values for MOS LNA

Author[Ref]	NF (dB)	Gain (dB)	IIP3 (dBm)	Power (mW)	F0 (GHz)
Shaeffer[7]	3.5	22	-9.5	30	1.5
Rafla[8]	2.5	22	-10	12	2.5
Huang[9]	3	19.8	4.5	22.4	2.4
Yang[10]	2.2	15	1.3	7.2	2.4
Tinella[11]	3	13.4	0	4.5	2.5
Wang[12]	1.6	12	8	20.62	2.5
Li[13]	2.88	15.9	-2.6/-11.2		2.45
Lagnado[14]	2.2	11	3	13.2	2.4

VII. CONCLUSION

In this paper, we have proposed a 2.4-2.5 GHz LNA with low power consumption. The LNA has been designed in a standard 0.13um CMOS technology. Good noise and gain performances were obtained at a low power consumption of only 7.33 mW. A noise Figure of 1.98 dB and a power gain of 20.343 dB were achieved for the proposed LNA. Also, a high IIP3 of 10 dBm, which shows the good linearity characteristics, was obtained

Table 2 . Summary of the proposed LNA performance

	Simulation Results
F0	2.4-2.5 GHz
power	7.33mW
NF	1.98dB
Gain	20.343 dB
Vdd	1.2V
IIP3	5dBm
S12	-44.69dB

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